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DERWENT-WEEK: 199233

TITLE: Wiring method for VLSI - using non-orthogonal wiring planes and using different die geometries for IC chips

PATENT-ASSIGNEE: ANONYMOUS[ANON]

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PATENT-FAMILY:

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APPLICATION-DATA:

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ABSTRACTED-PUB-NO: RD 339051A

BASIC-ABSTRACT:

The reduction is achieved in two ways: use of wiring planes at angles other than 90 deg.C and use of different die geometries for the integrated circuit chips. Either of these two techniques could be used by itself to achieve some reduction in wire length, but the best advantage is obtained by using them together. The wiring planes should be directed in angles that more uniformly cover all possible angles. Thus, if n wiring planes are to be used, they should be directed at angles that are multiples of 180 deg./n. To be specific, if 3 wiring planes are available, the wires should be at 0 deg. + 60 deg, and -60 deg.. For wires which must connect endpoints with a uniform angular distribution, the use of the 3 wiring planes results in a 13% decrease in the average wire length compared to the use of only x and y oriented wires.

Altering the die geometry of a chip does not in general alter the wiring length

for wires but can, however, very substantially alter the worst-case path length on the chip. (Such paths are generally the corner-to-corner **connections.**) The conventional chip geometry is square or rectangular with the sides parallel to the wiring directions. If one continues to use only x and y wiring, but dices the chips into diamonds, corner-to-corner wire length is decreased by 29% compared to that for a square with equal area. If one uses 3 wiring planes with wires at 0 deg, 60 deg. and -60 deg. and **hexagonal** dicing (**hexagons** can readily be packed to fill a plane, just as squares do), the worst-case wire length is reduced 38%.

ADVANTAGE - Shortens wires on integrated circuit chips. Increases speed, without any change in fabrication processes except for altering wafer dicing procedure.

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: WIRE METHOD VLSI NON ORTHOGONAL WIRE PLANE DIE GEOMETRY IC CHIP

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EPI-CODES: U11-C05D3; U11-G;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1992-210011

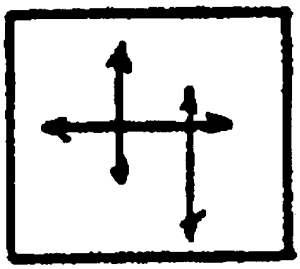

Fig. 1a

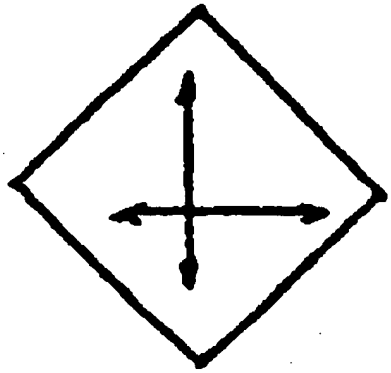

Fig. 1b

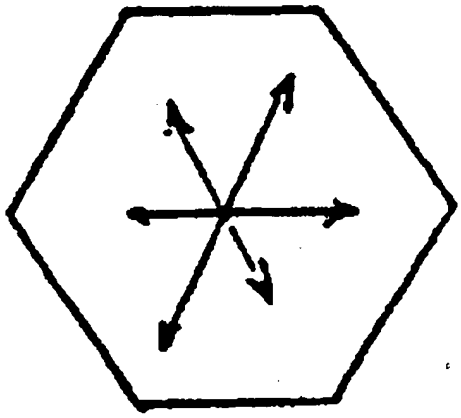

Fig. 1c